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10/068,004	02/08/2002	Woo Young So	1514.1010	6442

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/068,004	SO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-16,22 and 24-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16,22 and 24-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/3/06& 11/17/06*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on November 17, 2006 was filed after the mailing date of the first Office action on October 31, 2007. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. The amendment filed February 26, 2007 has been entered and new claims 29-34 have been added.

Response to Arguments

3. Applicant's arguments filed 2/26/2007 have been fully considered but they are not persuasive.

4. Applicants argue that the art rejection of independent claims 12 and 22 does not teach or suggest all the elements either explicitly or inherently. Specifically, Applicants argue that Yamazaki '190 does not disclose source and drain electrodes which respectively contact high-density source and drain regions without contact holes and that the Examiner's interpretation of the term "contact hole" is contrary to the accepted meaning of this term in the art which is a hole formed through an insulating layer to enable a source or drain to contact a source or drain region that is covered by the insulating layer by filling the contact hole with electrode material. Furthermore, Applicants argue that Yamazaki '190 does not disclose the first insulating layer or the gate insulating layer being an oxide as recited in claim 14.

5. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., contact hole which is a hole formed through an insulating layer to enable a source or drain to contact a source or drain region that is covered by the insulating layer by filling the contact hole with electrode material.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

6. In response to the argument that Yamazaki '190 does not disclose the first insulating layer or the gate insulating layer being an oxide, it is noted that Yamazaki discloses (first embodiment, figs. 2-5 and par. 45) that the gate insulating film is a silicon which undergoes a thermal oxidation. However, Yamazaki '190, as correctly pointed out by Applicants, is silent what gate insulating film 603 (second embodiment and figs. 6A-6D) is made of.

7. Applicants argue that the rejection of independent claim 12 based on the combined references of Zhang (US PG-Pub 2002/0105033) and Yamazaki '288 appears to be based on the Examiner's understanding that Zhang does not disclose how to connect electrodes to the source and drain regions 124 shown in fig. 10F of Zhang when Zhang does in fact disclose how to do this in figs. 6A-6D of Zhang. Furthermore, Applicants argue that the combination of Zhang and Yamazaki '288 is based on an improper hindsight.

8. In response, it is pointed out the rejection is not based on the Examiner's understanding that Zhang does not disclose how to connect electrodes to the source and drain regions 124 shown in fig. 10F of Zhang, rather it is based on the Examiner's understanding that figs. 10A-10F illustrate processes of manufacturing of TFTs according to an embodiment while figs. 6A-

6D show a structure of a TFT forming a pixel in an LCD device according to another embodiment. Therefore, the embodiment as detailed in figs. 10A-1F fails to disclose how to connect electrodes to the source and drain regions and one of ordinary skill in the art would be motivated to modify Zhang's device by incorporating electrodes connected to source and drain regions such as those taught by Yamazaki '288.

9. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 12, 15, 16, 26 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al ("Yamazaki") US PG-Pub 2004/0041190.

Yamazaki discloses in figs. 1-7 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 602 formed over said substrate having end portions; a first insulating layer

603 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 604 formed over said first insulating layer; a capping layer 605 formed over said gate electrode; spacers 608/701 formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 609/610 formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; low-density source and drain regions 611 having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers; and source and drain electrodes 614/615 which respectively contact said high density source and drain regions without contact holes -- note that contact holes which might have been formed previously do not exist in the final structure as they have been filled with electrode materials.

Regarding claims 15 and 16, Yamazaki discloses a silicide layer being formed between said source electrode and said high density source region and a silicide 704 between said drain electrode and said high density drain region; wherein said silicide layer comprise refractory metal **(as in claim 16)**.

Regarding claim 26, Yamazaki discloses in fig 6C said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Regarding claim 28, Yamazaki discloses said high-density source and drain regions being formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; and wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of semiconductor layer entirely under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers.

12. Claims 22, 24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

Yamazaki discloses in figs. 1-7 an active matrix display device, comprising: a substrate; a semiconductor layer 602 having end portions formed over said substrate; a first insulating layer 603 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 604 formed over said first insulating layer; a capping layer 605 formed over said gate electrode; spacers 608/701 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions 609/610 formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 611 having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers; source and drain electrodes 614/615 which respectively contact said high density source and drain regions -- note that contact holes which might have been formed previously do not exist in the final structure as they

have been filled with electrode materials; a planarization layer 349 having an opening portion which exposes a portion of one of said source and drain electrodes; and a pixel electrode 350 formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

Regarding claim 24, Yamazaki discloses a silicide layer 704 being formed between said source electrode and said high density source region and a silicide 704 between said drain electrode and said high density drain region

Regarding claim 27, Yamazaki discloses said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang ("Zhang") US PG-Pub 2002/0105033 in view of Yamazaki et al. USPN 5,568,288 ("Yamazaki '288").

Zhang discloses in figs. 10A-10F a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 104 formed over said substrate having end portions; a first insulating layer 106 disposed on said semiconductor layer so as to expose ones of the end portions of said

semiconductor layer; a gate electrode 108 formed over said first insulating layer; a capping layer (upper portion of region 109) formed over said gate electrode; spacers (portions of region 109 on both sidewall portions of gate electrode 108) formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 124n formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; low-density source and drain regions 114n/104f having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers, but lacks anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki '288 discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; and source and drain electrodes 102 which respectively contact high density source and drain regions 104/105 without contact holes.

Therefore, in view of Yamazaki '288, one having ordinary skill in the art at the time the invention was made would be motivated to modify Zhang's device by incorporating the teachings of Yamazaki so as to complete the thin film transistor as taught by Yamazaki '288.

Regarding claim 14, Zhang discloses said first insulating layer, said capping layer and said spacer are of an oxide.

15. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Yamazaki et al. US PG-Pub 2003/0207502 ("Yamazaki '502").

Yamazaki discloses (par. 4) the device structure as recited in the claim including an electro-optical device but does not specifically disclose an EL layer.

Yamazaki '502 discloses (par. 0343 and fig. 25) an organic electro-luminescence (EL) layer 4029 and a cathode electrode 4030 sequentially formed on a first predetermined area of a pixel electrode and on a second predetermined area of a planarization layer 4142.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Yamazaki '502 with Yamazaki so as to a realize a high efficiency integrated device.

16. Claims 12, 14 and 29-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teramoto et al. ("Teramoto") JP 7-78782 (cited in the IDS submitted under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 11/17/2006, see also equiv. USPN 5,962,897) in view of Yamazaki et al. JP 11-44892 ("Yamazaki '892").

Teramoto discloses in figs. 1 and 2 a thin film transistor (TFT), comprising: a substrate 11; a semiconductor layer 13 formed over said substrate having end portions; a first insulating layer 14 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 15 formed over said first insulating layer; a capping layer 16 formed over said gate electrode; spacers 22 formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions (17, 19) formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate

electrode and the capping layer; and source and drain electrodes (29, 30) which respectively said high-density source and drain regions without contact holes, but lacks anticipation of low-density source and drain regions under said spacers.

Yamazaki '892 discloses in fig. 6 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; and a low-density source and drain regions 611 having a same conductivity as high-density source and drain regions (609, 610) formed at regions of said semiconductor layer under spacers 608 between the gate electrode 604 and the high density source and drain regions 611, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

Therefore, in view of Yamazaki '892, one having ordinary skill in the art at the time the invention was made would be motivated to modify Teramoto's device by incorporating lightly doped drain (LDD) regions under said spacers. The motivation for doing so would be to minimize kink effect as taught by Yamazaki '892 (see abstract).

Regarding claim 14, Teramoto discloses (cols. 16 and 17, lines 14-33 and 19-25 respectively of equiv. USPN 5,962,897) said first insulating layer, said capping layer and said spacer are of an oxide.

Regarding claim 29, Teramoto discloses source and drain electrodes (29, 30) do not contact high-density source and drain regions (17, 19) via any electrode material filling any contact holes.

Regarding claim 30, Teramoto discloses the capping layer 16 and the spacers 22 being separate layers.

Regarding claim 31, Yamazaki '892 discloses source and drain electrodes (614, 615) do not contact a capping layer 605; and wherein the source and drain electrodes do not contact the spacers 608.

17. Claims 22 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teramoto in view of Yamazaki '892.

Teramoto discloses in figs. 1 and 2 an active matrix display device, comprising: a substrate; a semiconductor layer 13 having end portions formed over said substrate; a first insulating layer 14 formed over said semiconductor layer so as to expose end portions of said semiconductor layer; a gate electrode 15 formed over said first insulating layer; a capping layer 16 formed over said gate electrode; spacers 22 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions (17, 19) formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; source and drain electrodes (29, 30) which respectively contact said high density source and drain regions, but lacks anticipation of a low-density source and drain regions and a pixel electrode formed on a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes.

Yamazaki discloses in fig. 6 an active matrix display device, comprising: a substrate; a semiconductor layer 602 having end portions formed over said substrate; low-density source and drain regions 611 having a same conductivity as a high-density source and drain regions (609, 610) formed at entireties of off-set regions of said semiconductor layer entirely under spacers 608, thereby said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers; a planarization layer 349 having an opening portion which exposes a portion of one of

said source and drain electrodes; and a pixel electrode 350 formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

Therefore, in view of Yamazaki '892, one having ordinary skill in the art at the time the invention was made would be motivated to modify Teramoto's device by incorporating lightly doped drain (LDD) regions under said spacers. The motivation for doing so would be to minimize kink effect as taught by Yamazaki '892 (see abstract).

Regarding claim 32, Teramoto discloses source and drain electrodes (29, 30) do not contact high-density source and drain regions (17, 19) via any electrode material filling any contact holes.

Regarding claim 33, Teramoto discloses the capping layer 16 and the spacers 22 being separate layers.

Regarding claim 34, Yamazaki '892 discloses source and drain electrodes (614, 615) do not contact a capping layer 605; and wherein the source and drain electrodes do not contact the spacers 608.

Conclusion

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 11/17/2007 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANS
May 11, 2007

A. Sefer
Patent Examiner
Art Unit 2826